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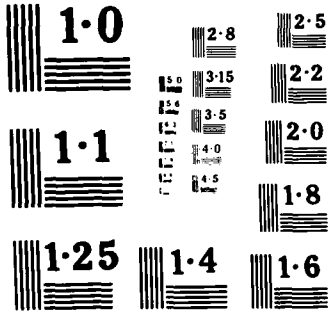

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REPORT SD-TR-85-96

AD-A163 117

Heavy-Ion Induced Single Event Upsets in a Bipolar Logic Device

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30 December 1985

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This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Heavy ion test results for a bipolar logic device of moderate complexity are presented in this report. Such devices require the implementation of special techniques for testing circuits of varying upset sensitivity, and unlike similar MOS devices, present problems with test data interpretation.

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PREFACE

We would like to take this opportunity to thank Professor John Choma of USC for many enlightening discussions concerning bipolar devices. In addition, we are grateful to Phil Grant, Sam Imamoto, Art Simoneau, and Bob Walter of The Aerospace Corporation for their help in the simulation effort, test hardware design and fabrication, and participation in the arduous data collection tasks. Special thanks to Norm Katz for his invaluable assistance in providing insight on the test-device circuit operation.

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FIGURES

TABLES

I. INTRODUCTION

This work was stimulated in part by the need to assess the vulnerability to single event upset of a computer that was to become part of a spacecraft control system. While previous investigations[1-5] have demonstrated that bipolar devices in general, and low-power Schottky ones in particular, tend to be sensitive to upsets in the space particle environment, the critical need for speed in certain applications mandates their use despite that shortcoming. In such cases, accurate knowledge of upset vulnerability of a microprocessor bit slice and the various support chips, or of a complete microprocessor system on a single chip is crucial for assessing the effectiveness of various measures implemented at the system level to circumvent the effects of single particle upsets.

At the present state of the art, such knowledge is derived from a detailed analysis of individual circuits on a given chip and from tests properly designed to measure the individual upset vulnerabilities of these circuits. It is possible that, at some levels of complexity such as that of microprocessor chips, there are circuit blocks that are completely inaccessible via any type of software. Upset predictions, in such cases, can only be obtained by means of modeling, unless special test chips can be manufactured.

It is an unfortunate, but nevertheless, real fact that reliable predictive models of bipolar circuits are nonexistent for all practical purposes, so that the development of special techniques for testing these complex devices takes on added importance. Some results of work along these lines have been published in the literature.[3,4] The present effort was undertaken in order to complement and extend the investigations of the AM2900-series device family still in progress at JPL.[6] We describe the results of this work to illustrate the techniques that must be developed and the results that are obtained in testing devices with a complexity level greater than that of a RAM or simple storage register.

II. TEST DEVICE CIRCUIT DESCRIPTION

In Fig. 1 is a block diagram of the AM2914 vectored priority interrupt encoder.[7] According to information provided by the manufacturer, elements sensitive to upset occur in the interrupt latches and the master/slave D flip-flops found in the various registers and other logic portions of the device. From discussions with AMD design engineers, we learned that two designs of the part were in existence. In the older version of the design, most of the vulnerable subcircuits were basically the same, except for one group associated with the slave latches of 18 master/slave D flip-flops. In Fig. 2 is a circuit diagram of one of these flip-flops, reproduced with the kind permission of AMD.[8] Recall that the base-collector drop across a saturated Schottky transistor is approximately 0.3 V and that the base-emitter drop at turn-on is about 0.7 V. Furthermore, note that because of elements not shown in Fig. 2, input low occurs at approximately 1.4 V, and that the device is operated at 5 V bias.

The four elements Q6-09 constitute the master latch and similarly the elements Q1-Q4, plus Q5, which serves as simple diode, form the slave. Note that the master circuit is quite symmetric in design with Q7 and Q9 forming a classic inverter pair, while the slave does not have that property. The division of the whole circuit into the master and slave portions can be appreciated best by noting that with the clock input high, the upper slave circuit is totally isolated from the input since both Q7 and Q9 are cut off.

Suppose now the clock input starts to go low. Whether Q7 or Q9 turns on first depends strictly on the state of the data (D) input. If D input is high, Q9 will turn on as soon as the input drops below about 3.9 V, and Q7 will remain off with its base at approximately 0.6 V. With the input low (1.4 V) and clock high, the base of Q7 is about 1.7 V, while the base of Q9 is 1.3 V and remains there regardless of the clock input state. Hence, on the downward transition of the clock when the D input is low, Q7 turns on while Q9 remains off. Data can be clocked in only on the downward transition of the clock, since once either Q7 or Q9 turns on, changing the level at the D input

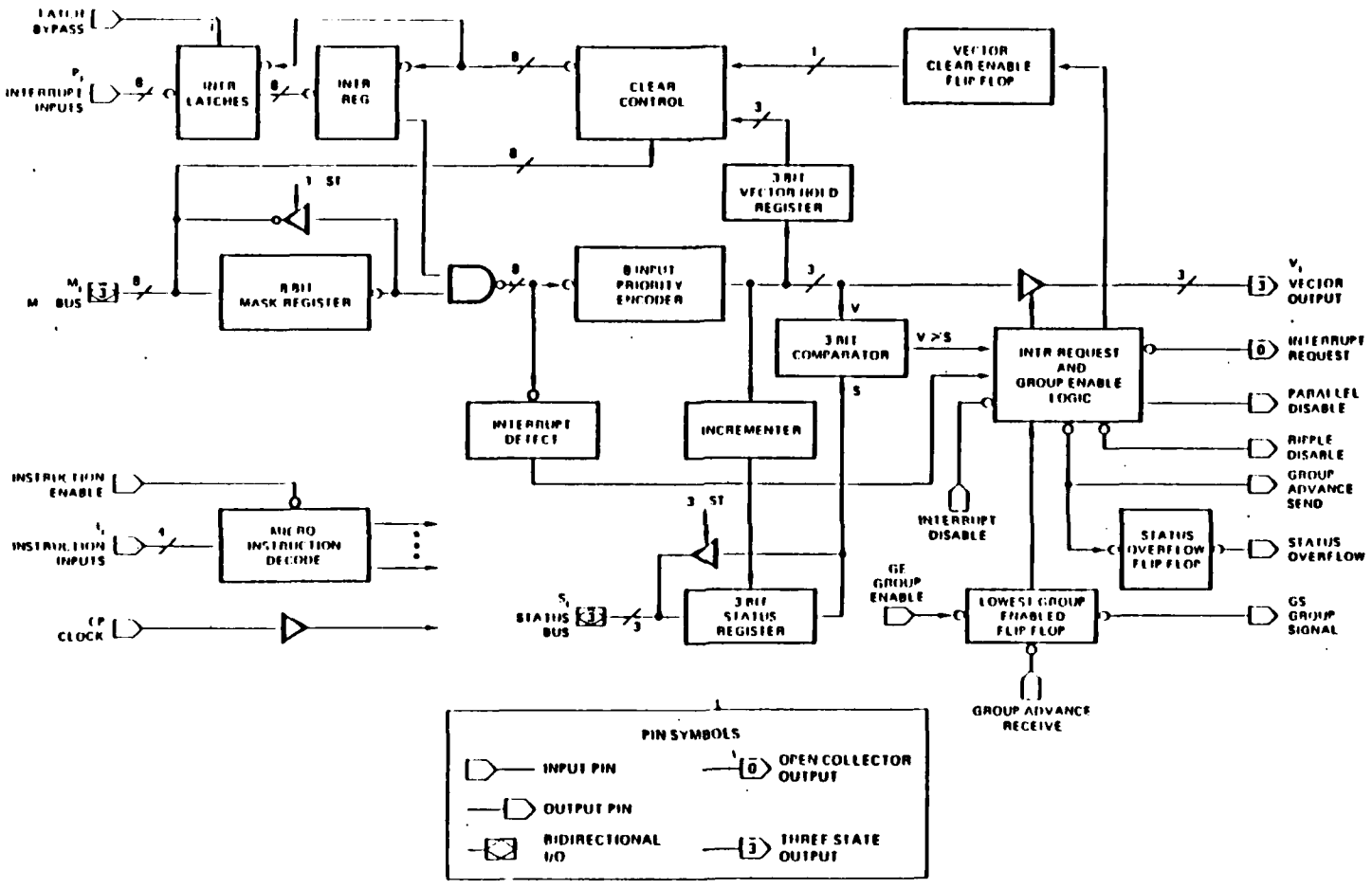

Fig. 1. Block Diagram of AM2914 Interrupt Encoder

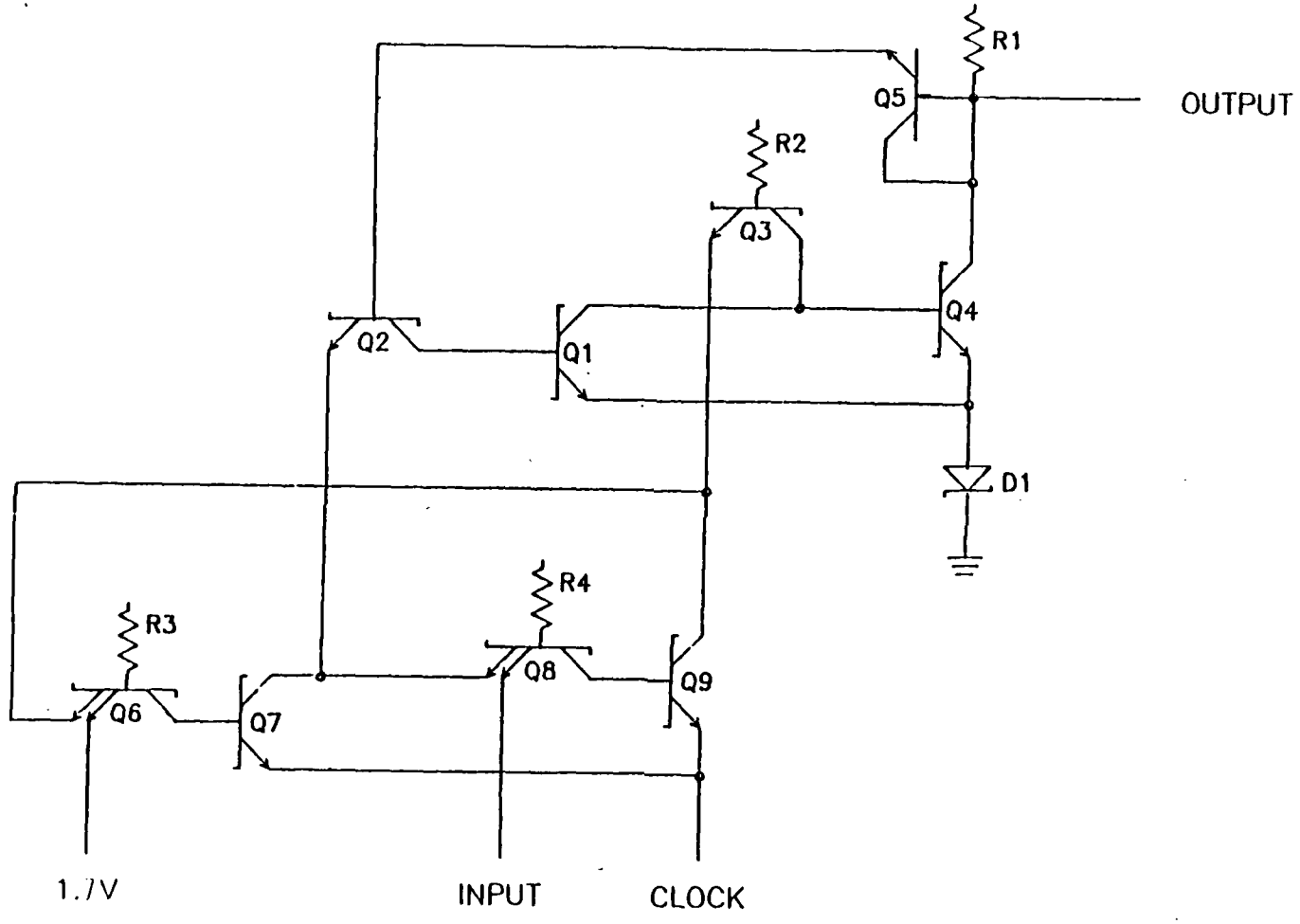

Fig. 2. Circuit Diagram of D Flip-Flop Cell in the AM2914 Mask Register

clearly has no effect on the rest of the circuit. It is easy to see that the output level follows the level clocked in, and that with the clock low, the transistor vulnerable to single event upset is Q7 or Q9, depending on whether or not it is off. When the clock input is high, Q1 and Q4 become the vulnerable transistors.

A somewhat bizarre situation develops when the clock is high and output is low. In that case Q5, which acts as an ordinary diode, is barely able to conduct, if at all, so that the base of Q2 is near 0V while the emitter is high. Since Q1 is off, its base, together with the collector of Q2, are floating. Any holes injected at the base of Q1 will be quite effective in raising the base potential since there is no leakage path available. We might expect therefore that less charge is needed at the base of Q1 to turn it on (and,hence,turn Q4 off), than in the case of a particle hit on Q4 in the off state. In the latter case, Q1 is on and provides an alternate path to ground for the resulting current. On an intuitive basis it therefore appears reasonable that the critical charge for causing a low-to-high transition with the clock high should be significantly less than a high-to-low. Engineers at AMD have informed us that they had experienced problems because of this feature of the circuit, and that these problems had been cured by a design change in the more recent version of the device, where a second emitter in Q2 is returned to the collector of Q4. In view of the above situation, it appeared that in the old version of the device, at least two values of upset thresholds could be expected in the heavy ion tests, with one significantly lower than the rest. Here we report on the test results obtained with this older part type.

III. INSTRUMENTATION AND TEST METHOD

Since we have previously described the general techniques of testing microcircuits with heavy ions,[9] we limit our present discussion primarily to methods specifically applicable to the AM2914. In Table 1 are shown the ions used in the experiments, together with their respective energies just before striking the chip surface. Also, included in the table is the linear charge density (LCD) along the track, computed from the known value of linear energy transfer (LET) at the incident beam energy. Particles with intermediate values of LCD were simulated by rotating the chip to obtain oblique angles of incidence and assuming that the resulting increase in path length through the sensitive region had the same effect as a comparable fractional increase in LCD. Figure 3, reproduced from Ref. 9, shows the test instrumentation in schematic form.

Delidded parts under test were placed on a special board inside the vacuum chamber. (Since the particles used in these tests have very short range in air, all testing must be done in vacuum with delidded devices.) A controller in the form of a microcomputer (μC in Fig. 3) was located outside and next to the chamber, in order to minimize cable length between the test board and the controller. Instructions were sent to the controller, and data from it were received by means of a Silent 700 teletype terminal.

Immediately prior to any given exposure, a single chip was positioned in the path of the beam and oriented at a desired angle by remote control. Next, the controller was commanded to begin exercising the chip by means of a program stored in PROM. Following a check of appropriate beam-monitor data and proper chip operation, the exposure was started by opening the remotely controlled beam flap directly in front of the chip. During the exposure, an approximate real-time count of all upsets, regardless of their origin, was kept in a special monitor. The total ion fluence was also measured by counting the pulses from the scintillation-counter monitor, as shown in Fig. 3. When an appropriate number of errors was detected, or a desired fluence achieved, the exposure was terminated by closing the shutter and halting the device-exercise program. Upset data were detected and stored in memory during the exposure and saved for further analysis.

Table 1. Properties of Heavy Ions Used in Device Bombardment

Ion Species	Atomic Number	Energy (MeV)	LET (MeV cm^2/mg)	Linear Charge Density (pC/μm)
Oxygen	8	104	3.1	0.03
		32	5.7	0.06
Argon	18	160	15.4	0.15
Krypton	36	140	40	0.5

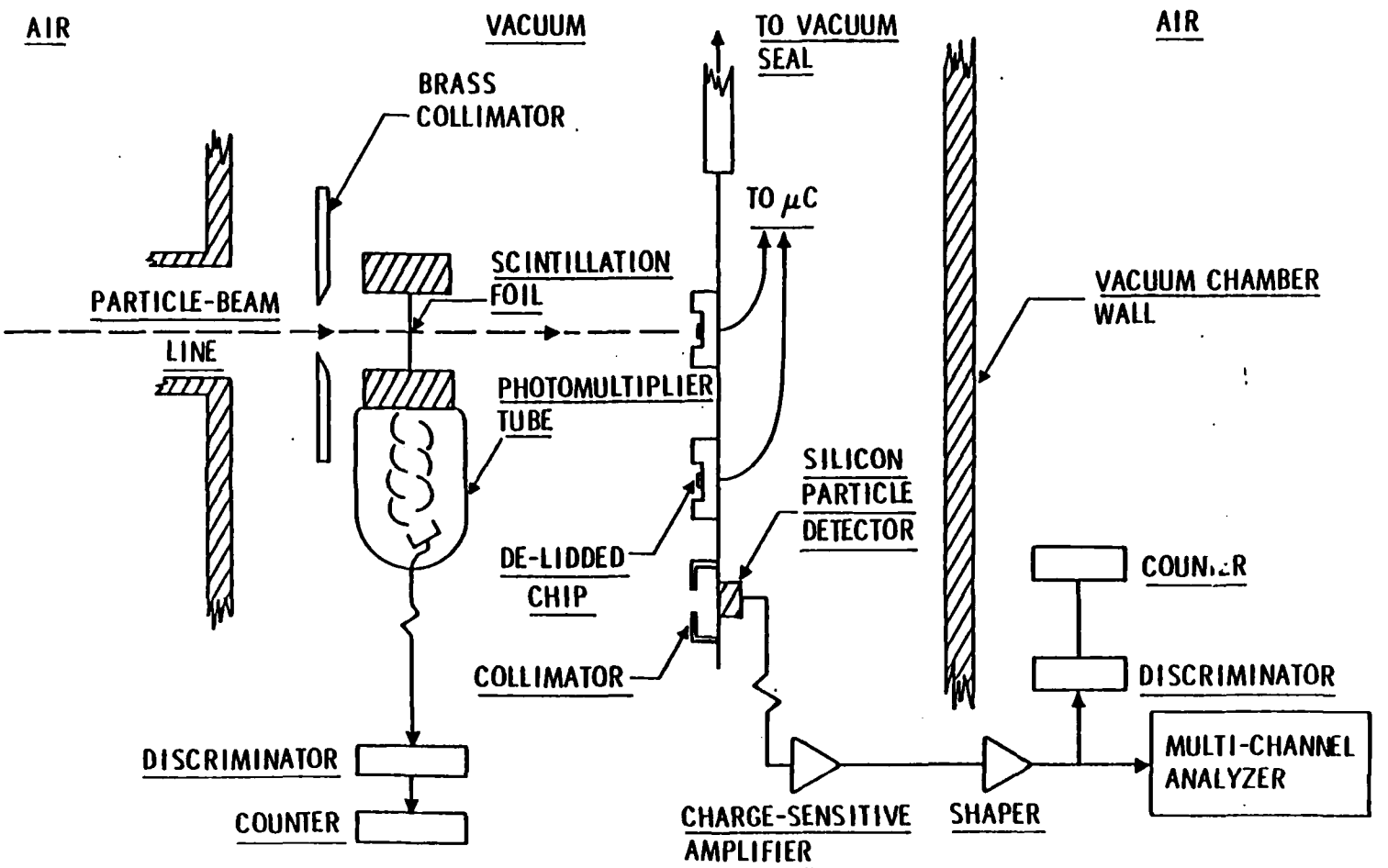

Fig. 3. Schematic Representation of Test Hardware

The test control software was written in the form of a group of basic subprograms that could be linked in various sequences within the main program, depending on the individual test requirements. Analysis of the device specifications and discussions with AMD engineering staff had convinced us that tests of the mask and status registers would be sufficient to characterize the device completely. The mask register contained strong master and weak slave latches, while in the status register both latch types were strong. Furthermore, both of the above registers were quite amenable to testing from the point of view of control software requirements. The terms strong and weak refer to the relative magnitude of the upset threshold inferred above from analysis of the respective latch circuits. The four subprograms and functions they perform in the case of the mask register are summarized in Table 2. A similar set of subprograms applies to the tests of the status register.

During the heavy ion experiment, the main program started a timer and executed the subroutine S1 first. The subroutine S1 initially set the D flip-flop output to 1 and kept the clock line low for 1 sec during which upsets could occur. After 1 sec, the state of the D flip-flop output was checked. It differed from 1, an error counter was incremented by 1 and the error location was stored in computer memory. Each of the other subroutines shown in Table 2 was executed in similar fashion during 1-sec intervals, followed by a similar set of tests using subroutines for testing the status register. The complete sequence was automatically repeated by the computer and terminated either by a preset beam-monitor counter, a timer, or by hand, depending on the individual test requirements.

Table 2. Summary of Subprograms for Testing the Mask Register

Static Conditions		SEU Observation	Program Subroutines
Output of D F/F	Clock Line		
1	0	1 to 10 transition of the slave	S1
0	0	0 to 10 transition of the slave	S1
1	0	1 to 10 transition of the master	S3
0	1	0 to 1 transition of the master	S4

IV. RESULTS

The status register test results are shown in Fig. 4 for both the master and the slave where the upset cross-section is plotted versus LCD. No upsets were observed at LCDs below 0.1 pC/μm, and for both latches, the cross-section reaches the value between 2000 and 4000 μm^2 at or slightly above 0.2 pC/μm. Within statistical errors indicated by bars in the figure, the master and slave results are the same.

In the case of the mask register data, as shown in Fig. 5, the threshold and cross-section for the master resemble the status register data. The slave of the mask register flip-flop, however, has an LCD threshold between a factor of two and four less than the other latches.

The gap in the data between 0.1 and 0.2 pC/μm is caused by a lack of overlap between charge deposits obtained at large singles with the 30 MeV oxygen beam and normally incident argon beam. At the time these tests were performed, time was not available for bombardment by particles with an intermediate value of LCD.

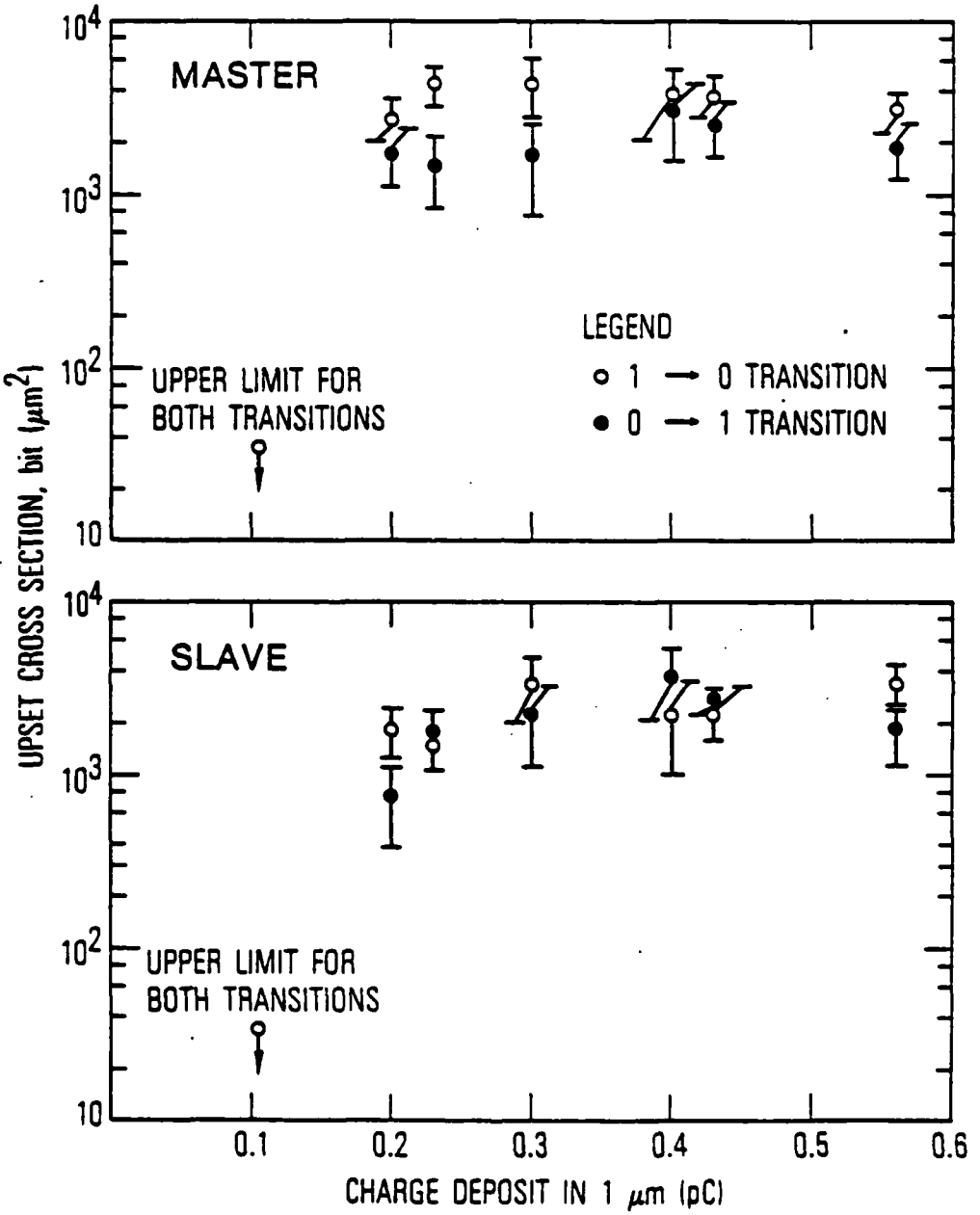

Fig. 4. Upset Data for AM2914 Status Register

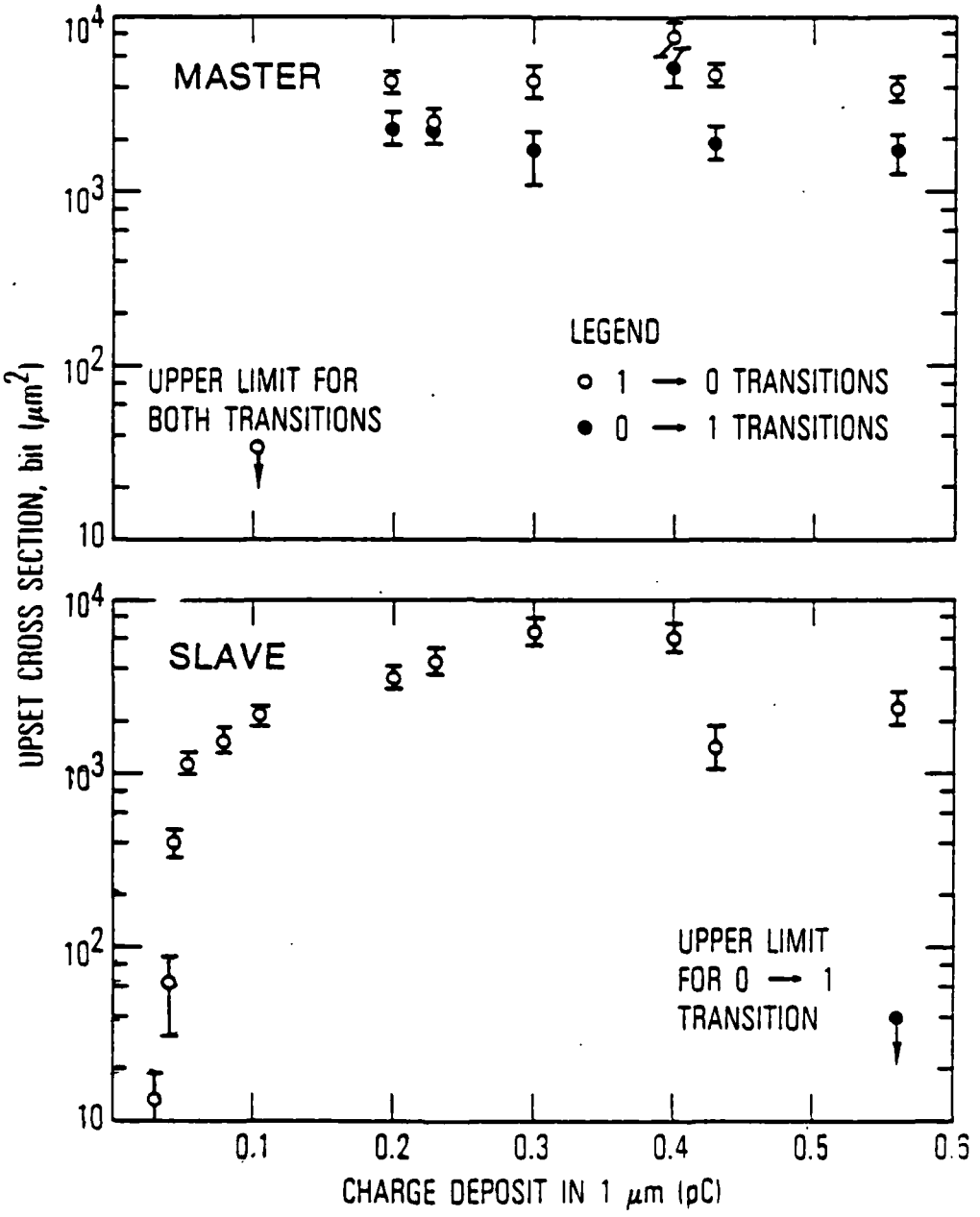

Fig. 5. Upset Data for AM2914 Mask Register

V. DISCUSSION

It is clear that the results agree qualitatively with the predictions based on the intuitive analysis of the circuit in Fig. 2. However, the lack of 0 to 1 upsets in the mask register slave, as well as the values of the observed values of the upset cross-section near and above the LCD threshold warrant further discussion, as do the values of the LCD threshold itself.

A cross-section of a typical transistor involved in the upset process drawn roughly to scale is shown in Fig. 6. There are some differences between individual transistors, and data on the exact geometry are not readily obtainable, but for purposes of this discussion, the information in the figure is sufficient. We shall assume that the dimensions in and out of the paper are the same. The complexity of this bipolar element relative to an MOS transistor is readily apparent from this figure. A priori, there appear to be three depletion regions in the off transistor, which are potential sources of single event upsets. These are the depletion regions around the p-type base diffusion together with the Schottky barrier and the n-type epi-layer of the collector region, the considerably wider depletion layer between the collector and the high resistivity p-subtrate, and finally the layer between the heavily doped p^+ isolation layer and collector epi-layer.

The geometrical area of the base diffusion is approximately 500 μm^2. A glance at the upset cross-section data in Figs. 4 and 5 show that the measured cross-sections exceed 2000 μm^2 at large LCD. This suggests that most of the action occurs around the buried layer region whose area is in the 4000 μm^2 range. Another argument supporting that interference is the fact that the depletion region in the highly doped substrate is quite wide. Furthermore, because of the high resistivity of the substrate, any funneling that may exist here will be greatly enhanced over a similar effect near the base junction where the epi-layer doping density is in excess of 10 times that in the substrate. The collector-isolation junction would not appear to contribute significantly to the upset cross-section, since if it did, a pronounced pedestal would presumably appear just below the main threshold. However, the resolution in the data is such that this effect cannot be ruled out.

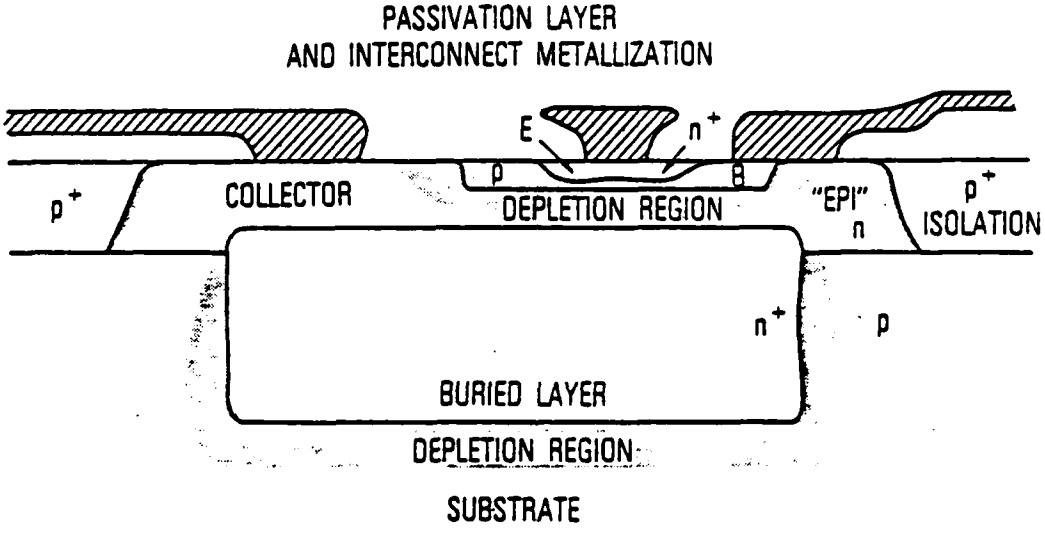

Fig. 6. Cross-Section of Buried Layer TTL Transistor

There are valid objections to the above plausible-sounding arguments, which must be considered. First is the fact that while it may be true that up to about 10 times more charge (including funneling) may be produced near the substrate than the base, a current source between the collector and base should be much more effective in producing regenerative action than one between the collector and substrate. In the former case, the lesser value of the current is multiplied by the transistor β, an effect which should easily compensate for the lesser amount of current injected into the base. The area enhancement may be simply caused by holes generated in the collector epi-layer portions away from the depletion region, which are collected in the base by diffusion. The diffusion time may be reduced by the device geometry to the point where there is sufficient current to turn on the transistor. Effects of geometry on charge collected by diffusion have been recently discussed in the literature[10] and should be carefully considered in any quantitative models of devices such as the one under discussion.

So far we have not been able to find a plausible explanation as to why upsets in both directions occur in the master, while in the slave, only 1 to 0 transitions are observed. This phenomenon is probably related to the strong asymmetry in the slave latch, and its explanation requires a detailed quantitative analysis of the circuit. Simulations using the SPICE program have been attempted on the circuits using various and sundry parameters. Various and sundry results were obtained using these parameters, which is not surprising. Perhaps the most significant result of the simulation effort has been the realization of how rudimentary our knowledge is in this field, and how much remains to be done before, if ever we acquire the ability to deduce realistic circuit parameters of an active bipolar device from a knowledge of its physical design.

VI. SUMMARY AND CONCLUSIONS

Results of heavy ion tests on a bipolar, low power Schottky microcircuit device agree with predictions based on a qualitative analysis of subcircuits contained in this device. These tests were able to individually determine the upset vulnerability of two independent subcircuits present on the chip. Despite this agreement, the results raise numerous questions when examined in light of the relatively complex device geometry and physical properties. To the best of our knowledge, no reliable models exist that can predict with any degree of credibility the upset rate of bipolar devices from a knowledge of the device circuit parameters, either obtained empirically from electrical tests or calculated on the basis of geometry and physical process features. Consequently, the only current reliable way to assess device vulnerability to single event upsets is by direct measurement of the LCD or LET threshold together with the upset cross-section using heavy ions and by bombardment with energetic protons (50 MeV or more) where proton-induced upsets are of concern.

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